REMARKS

In response to the Office Action mailed March 22, 2005, Applicants respectfully request reconsideration. Claims 1-7 were previously pending in this application. Claims 1-6 have been amended. New claims 10-16 have been added. As a result, claims 1-7 and 10-16 are pending for examination with claims 1 and 10 being independent. No new matter has been added.

Objections to the Specification

The Office Action objects to the Abstract for containing a relative term "possibly". The Abstract has been amended to delete the term "possibly" and is now in accordance with MPEP § 608.01(b).

Accordingly, withdrawal of this objection is respectfully requested.

Rejections under 35 U.S.C. §112

The Office Action rejects claims 1-7 under 35 U.S.C. §112 second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

The Office Action rejects claim 1 for containing a relative term "possibly" and for not proving antecedent basis for the phase "thin wafer". The Office Action also rejects the limitation "forming connections between different areas" for lacking clarity. Claim 1 has been amended to delete the term "possibly" and the phrase "thin wafer" has been amended to "thin semiconductor wafer" to provide antecedent basis. The limitation "forming connections between different areas" has been amended to "forming interconnections between opened areas" for the purpose of clarity.

The Office Action rejects claim 2 for failing to further limit claim 1 with a method limitation. Claim 2 has been amended to clearly recite an insulating layer.

The Office Action rejects claim 3 for not positively reciting a step of forming an insulating layer. Claim 2 has been amended to clearly introduce the insulating layer.

The Office Action rejects claim 4 for not providing antecedent basis for "areas of reduced thickness" and for improperly making a comparison with "like said openings". Claim 4 has been amended to provide antecedent basis for the phrase "areas of reduced thickness" and the phrase "like said openings" has been deleted.

The Office Action rejects claim 5 for not providing antecedent basis for the phrase "bottom of the openings". The Office Action also rejects claim 5 for not clearly defining an insulating layer. The phrase "bottom of the openings" has been amended to "the open areas" and claim 2 has been amended to properly introduce an insulating layer.

The Office Action also rejects claim 5 for not clearly explaining a presence of silicon to be annealed to form silicide. Applicants respectfully disagree. The specification clearly describes the annealing step used to form silicide. As described by the specification (page 8, lines 3-8), a metal is deposited in a first phase on the side of the insulating layer. In a second phase, an anneal is performed to form a silicide layer 70 at the bottom of opening Op3 previously formed in insulating layer D1. Then, in a last phase, the metal which has not been turned into silicide is removed. Applicants respectfully submit claim 5 properly describes the invention as written in the specification.

The Office Action rejects claim 6 for containing the relative term "possibly" and for not providing antecedent basis for "after the step of filling the openings and possibly the areas of reduced thickness". The Office Action also rejects to claim 6 for containing a contradicting limitation. Claim 6 has been amended to delete the term "possibly". Claim 6 has also been amended to clarify "gluing the third support wafer..." in order to clarify the contradicting limitations. Claim 4 has been amended to provide antecedent basis for "after the step of filling the openings and possibly the areas of reduced thickness".

Applicants not that the amendments to claims 1-6 have been made for clarification only and do not narrow the scope of the claims.

Accordingly, withdrawal of the rejection of claims 1-7 under 35 U.S.C. §112 is respectfully requested.

Rejections Under 35 U.S.C. §102

The Office Action rejects claims 1-7 under 35 U.S.C. §102 as purportedly being anticipated by Gaul et al., U.S. Patent No. 5,807,783 (Gaul). Applicants respectfully traverse this rejection.

Gaul illustrates an integrated circuit and a method for fabricating the integrated circuit (Col. 2, lines 37-39). The method for fabricating the integrated circuit, as described by Gaul, is depicted in figures 2-8 (relied upon by the Office Action). The device described by Gaul includes a handle wafer 12 bonded to a rear surface of a semiconductor device wafer 10 with use of an oxide bond layer 14 (Col. 4, lines 13-16). A second handle wafer 40 is later bonded to an interconnect layer 30 which is on an upper surface of semiconductor device wafer 10 (Col. 5, lines 4 and 5). The handle wafer 12 is later removed and external contacts 36 are then provided in order to contact conductive material 33 in vias as well as bottomed out diffusions 21 and 22 (Col. 6, lines 32-34 and Col. 5, lines 45-47).

By contrast, amended claim 1 is directed towards a method for manufacturing buried connections in an integrated circuit comprising providing a structure formed of a first support wafer glued onto a rear surface of a thin semiconductor wafer, one or several elements of the integrated circuit being formed in and above the thin semiconductor wafer, gluing a second support wafer on the structure on a front surface side of the thin semiconductor wafer, removing the first support wafer, forming interconnections between opened areas of the rear surface of the thin semiconductor wafer, gluing a third support wafer on the interconnections, and removing the second support wafer.

Gaul does not teach or suggest gluing a third *support wafer* on the interconnections, as recited in claim 1. As described above, Gaul instead teaches providing external contacts. No where in Gaul are the external contacts 36 described as a "support wafer". In fact, as described in column 5, lines 54 and 55, external contacts 36 are used to connect the internal contacts to external electrical circuits. Therefore, Applicants respectfully submit that the Office Action misinterprets the external contacts described by Gaul. Clearly, external contacts are not a support wafer. Therefore, Gaul does not teach or suggest gluing a third *support wafer* on the interconnections, as recited in claim 1.

Accordingly, claim 1 distinguishes over Gaul and withdrawal of the rejection under 35 U.S.C. §102 is respectfully requested.

Claims 2-7 depend from claim 1 and are allowable for at least the same reasons.

Claim 10 is directed towards a method for manufacturing buried connections in an integrated circuit comprising attaching a first support wafer to a first surface of a thin semiconductor wafer, attaching a second support wafer to a second surface of the thin semiconductor wafer, removing the first support wafer, forming interconnections between opened areas of the first surface of the thin semiconductor wafer, attaching a third support wafer to the interconnections, and removing the second support wafer.

As should be appreciated from the above discussion relating to claim 1, Gaul does not teach or suggest attaching a third *support wafer* to the interconnections, as recited by claim 10.

Claims 11-16 depend from claim 10 and are allowable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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